Thu, 20 Jul 2006, 1:49:58 PM EST

Edit an existing query or compose a new query in the Search Query Display.

Select a search number (#) to:

- Add a query to the Search Query Display
- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

Search Query Display

Recent Search Queries

#1 ((gate circuit? and crosstalk and delay)<in>metadata)

#2 gate<sentence>circuit? and crosstalk and delay

#3 ((gate<sentence>circuit? and crosstalk and delay)<AND>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata))

#4 ((((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)))
<AND>((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)) and
aggressor)

#5 ((((((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)))
<and>((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)) and
aggressor))<AND>((((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)))
<and>((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)) and
aggressor) and crosstalk<sentence>delay)

#6 ((((((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)))
<and>((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)) and
aggressor))<AND>((((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)))
<and>((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)) and
aggressor) and crosstalk<sentence>delay)

#7 ((((((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)))
<and>((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)) and
aggressor))<AND>((((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)))
<and>((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)) and
aggressor) and crosstalk<sentence>delay)

#8 ((((((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)))
<and>((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)) and
aggressor))<AND>((((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)))
<and>((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)) and
aggressor) and crosstalk<sentence>delay)

#9 ((((((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)))
<and>((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)) and
aggressor))<AND>((((gate<sentence>circuit? and crosstalk and delay)<and>

(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)))
<and>((gate<sentence>circuit? and crosstalk and delay)<and>
(gate<sentence>circuit? and crosstalk and delay and model*<in>metadata)) and
aggressor) and crosstalk<sentence>delay)

[redacted]

Results for "((gate circuit? and crosstalk and delay)<in>metadata)"

Your search matched 0 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

View Session History

New Search

Modify Search

((gate circuit? and crosstalk and delay)<in>metadata) Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

No results were found.

Please edit your search criteria and try again. Refer to the Help pages if you need assistance revising your search

Results for "((((((gate<sentence>circuit? and crosstalk and delay)<and>(gate<sentence>circuit? ..." e-mail

Your search matched 34 of 46 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

View Session History

New Search

Modify Search

((((((gate<sentence>circuit? and crosstalk and delay)<and>(gate<sentence>circuit? Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

view selected items Select All Deselect All

1. **Analytical modeling and characterization of deep-submicrometer interconnect**
Sylvester, D.; Chenming Wu;
Proceedings of the IEEE
Volume 89, Issue 5, May 2001 Page(s):634 - 664
Digital Object Identifier 10.1109/5.929648
AbstractPlus | References | Full Text: PDF(524 KB) | Full Text: HTML IEEE JNL
Rights and Permissions

2. **Crosstalk delay analysis of a 0.13-/spl mu/m node test chip and precise gate-level simulatior**
Sasaki, Y.; Sato, M.; Kuramoto, M.; Kikuchi, F.; Kawashima, T.; Masuda, H.; Yano, K.;
Solid-State Circuits, IEEE Journal of
Volume 38, Issue 5, May 2003 Page(s):702 - 708
Digital Object Identifier 10.1109/JSSC.2003.810062
AbstractPlus | References | Full Text: PDF(502 KB) IEEE JNL
Rights and Permissions

3. **Eliminating false positives in crosstalk noise analysis**
Ran, Y.; Kondratyev, A.; Tseng, K.H.; Watanabe, Y.; Marek-Sadowska, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 24, Issue 9, Sept. 2005 Page(s):1406 - 1419
Digital Object Identifier 10.1109/TCAD.2005.850829
AbstractPlus | Full Text: PDF(496 KB) IEEE JNL
Rights and Permissions

4. **Static timing analysis for level-clocked circuits in the presence of crosstalk**
Hassoun, S.; Cromer, C.; Calvillo-Gamez, E.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 22, Issue 9, Sept. 2003 Page(s):1270 - 1277
Digital Object Identifier 10.1109/TCAD.2003.816209
AbstractPlus | References | Full Text: PDF(427 KB) IEEE JNL
Rights and Permissions

5. **Crosstalk noise reduction in synthesized digital logic circuits**
Milter, O.; Kolodny, A.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 11, Issue 6, Dec. 2003 Page(s):1153 - 1158
Digital Object Identifier 10.1109/TVLSI.2003.817551

AbstractPlus | References | Full Text: PDF(439 KB) IEEE JNL
Rights and Permissions

6. **Bidirectional closed-form transformation between on-chip coupling noise waveforms and in change curves**
Sato, T.; Yu Cao; Agarwal, K.; Sylvester, D.; Chenming Hu;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 22, Issue 5, May 2003 Page(s):560 - 572
Digital Object Identifier 10.1109/TCAD.2003.810750
AbstractPlus | References | Full Text: PDF(622 KB) IEEE JNL
Rights and Permissions

7. **Cancellation of crosstalk-induced jitter**
Buckwalter, J.F.; Hajimiri, A.;
Solid-State Circuits, IEEE Journal of
Volume 41, Issue 3, March 2006 Page(s):621 - 632
Digital Object Identifier 10.1109/JSSC.2005.864113
AbstractPlus | Full Text: PDF(2000 KB) IEEE JNL
Rights and Permissions

8. **Driver modeling and alignment for worst-case delay noise**
Blaauw, D.; Sirichotiyakul, S.; Oh, C.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 11, Issue 2, April 2003 Page(s):157 - 166
Digital Object Identifier 10.1109/TVLSI.2002.808448
AbstractPlus | References | Full Text: PDF(411 KB) IEEE JNL
Rights and Permissions

9. **Crosstalk in VLSI interconnections**
Vittal, A.; Chen, L.H.; Marek-Sadowska, M.; Kai-Ping Wang; Yang, S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 18, Issue 12, Dec. 1999 Page(s):1817 - 1824
Digital Object Identifier 10.1109/43.811330
AbstractPlus | References | Full Text: PDF(408 KB) IEEE JNL
Rights and Permissions

10. **The challenge of signal integrity in deep-submicrometer CMOS technology**
Caignet, F.; Delmas-Bendhia, S.; Sicard, E.;
Proceedings of the IEEE
Volume 89, Issue 4, April 2001 Page(s):556 - 573
Digital Object Identifier 10.1109/5.920583
AbstractPlus | References | Full Text: PDF(836 KB) | Full Text: HTML IEEE JNL
Rights and Permissions

11. **Delay calculation capturing crosstalk effects due to coupling capacitors**
Cho, K.;
Electronics Letters
Volume 41, Issue 8, 14 April 2005 Page(s):458 - 460
Digital Object Identifier 10.1049/el:20050127
AbstractPlus | Full Text: PDF(176 KB) IEE JNL

12. **Static transition probability analysis under uncertainty**
Garg, S.; Tata, S.; Arunachalam, R.;
Computer Design: VLSI in Computers and Processors, 2004. ICCD 2004. Proceedings. IEEE Inten on
11-13 Oct. 2004 Page(s):380 - 386
Digital Object Identifier 10.1109/ICCD.2004.1347950
AbstractPlus | Full Text: PDF(296 KB) IEEE CNF
Rights and Permissions

☐ **13. Worst case crosstalk noise for nonswitching victims in high-speed buses**
Jun Chen; Lei He;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 24, Issue 8, Aug. 2005 Page(s):1275 - 1283
Digital Object Identifier 10.1109/TCAD.2005.850823
AbstractPlus | Full Text: PDF(376 KB) IEEE JNL
Rights and Permissions

☐ **14. Noise-aware interconnect power optimization in domino logic synthesis**
Ki-Wook Kim; Seong-Ook Jung; Narayanan, U.; Liu, C.L.; Sung-Mo Kang;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 11, Issue 1, Feb. 2003 Page(s):79 - 89
Digital Object Identifier 10.1109/TVLSI.2002.801630
AbstractPlus | References | Full Text: PDF(715 KB) IEEE JNL
Rights and Permissions

☐ **15. Analog macromodeling for combined resistive vias, resistive bridges, and capacitive crosst**
Chary, S.; Bushnell, M.L.;
VLSI Design, 2006. Held jointly with 5th International Conference on Embedded Systems and Desi
Conference on
3-7 Jan. 2006 Page(s):6 pp.
Digital Object Identifier 10.1109/VLSID.2006.47
AbstractPlus | Full Text: PDF(184 KB) IEEE CNF
Rights and Permissions

☐ **16. Nonlinear driver models for timing and noise analysis**
Tutuianu, B.; Baldick, R.; Johnstone, M.S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 23, Issue 11, Nov. 2004 Page(s):1510 - 1521
Digital Object Identifier 10.1109/TCAD.2004.835136
AbstractPlus | References | Full Text: PDF(656 KB) IEEE JNL
Rights and Permissions

☐ **17. A concurrent fault simulation for crosstalk faults in sequential circuits**
Phadoongsidhi, M.; Le, K.T.; Saluja, K.K.;
Test Symposium, 2002. (ATS '02). Proceedings of the 11th Asian
18-20 Nov. 2002 Page(s):182 - 187
Digital Object Identifier 10.1109/ATS.2002.1181708
AbstractPlus | Full Text: PDF(286 KB) IEEE CNF
Rights and Permissions

☐ **18. A method to estimate slew and delay in coupled digital circuits**
Batterywala, S.; Shenoy, N.;
VLSI Design, 2003. Proceedings. 16th International Conference on
4-8 Jan. 2003 Page(s):411 - 416
Digital Object Identifier 10.1109/ICVD.2003.1183170
AbstractPlus | Full Text: PDF(312 KB) IEEE CNF
Rights and Permissions

☐ **19. Non-iterative switching window computation for delay-noise**
Thudi, B.; Blaauw, D.;
Design Automation Conference, 2003. Proceedings
2-6 June 2003 Page(s):390 - 395
AbstractPlus | Full Text: PDF(763 KB) IEEE CNF
Rights and Permissions

☐ **20. Modeling crosstalk in resistive VLSI interconnections**

Vittal, A.; Hui Chen, L.; Marek-Sadowska, M.; Kai-Ping Wang; Yang, S.;
VLSI Design, 1999. Proceedings. Twelfth International Conference On
7-10 Jan. 1999 Page(s):470 - 475
Digital Object Identifier 10.1109/ICVD.1999.745200

AbstractPlus | Full Text: PDF(92 KB) IEEE CNF
Rights and Permissions

☐ **21. Timing analysis with crosstalk is a fixpoint on a complete lattice**
Hai Zhou;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 22, Issue 9, Sept. 2003 Page(s):1261 - 1269
Digital Object Identifier 10.1109/TCAD.2003.816211

AbstractPlus | References | Full Text: PDF(413 KB) IEEE JNL
Rights and Permissions

☐ **22. Crosstalk-induced jitter equalization**
Buckwalter, J.; Hajimiri, A.;
Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005
18-21 Sept. 2005 Page(s):409 - 412
Digital Object Identifier 10.1109/CICC.2005.1568692

AbstractPlus | Full Text: PDF(416 KB) IEEE CNF
Rights and Permissions

☐ **23. Power consumption in point-to-point interconnect architectures**
Ortiz, A.G.; Murgan, T.; Indrusiak, L.; Glesner, M.;
Integrated Circuits and Systems Design, 2002. Proceedings. 15th Symposium on
9-14 Sept. 2002 Page(s):155 - 160
Digital Object Identifier 10.1109/SBCCI.2002.1137652

AbstractPlus | Full Text: PDF(371 KB) IEEE CNF
Rights and Permissions

☐ **24. Noise-aware driver modeling for nanometer technology**
Xiaoling Bai; Chandra, R.; Dey, S.; Srinivas, P.V.;
Quality Electronic Design, 2003. Proceedings. Fourth International Symposium on
24-26 March 2003 Page(s):177 - 182
Digital Object Identifier 10.1109/ISQED.2003.1194728

AbstractPlus | Full Text: PDF(665 KB) IEEE CNF
Rights and Permissions

☐ **25. Analytical models for crosstalk excitation and propagation in VLSI circuits**
Wei-Yu Chen; Gupta, S.K.; Breuer, M.A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 21, Issue 10, Oct. 2002 Page(s):1117 - 1131
Digital Object Identifier 10.1109/TCAD.2002.802276

AbstractPlus | References | Full Text: PDF(422 KB) IEEE JNL
Rights and Permissions

Results for "((((((gate<sentence>circuit? and crosstalk and delay)<and>(gate<sentence>circuit? ..." e-mail

Your search matched 34 of 46 documents.

A maximum of 34 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

View Session History

New Search

Modify Search

((((((gate<sentence>circuit? and crosstalk and delay)<and>(gate<sentence>circuit? a Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

view selected items Select All Deselect All

26. **Noise library characterization for large capacity static noise analysis tools**
Gyure, A.; Kasnavi, A.; Lo, S.; Tehrani, P.F.; Shu, W.; Shahram, M.; Wang, J.W.; Zedja, J.;
Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium on
21-23 March 2005 Page(s):28 - 34
Digital Object Identifier 10.1109/ISQED.2005.85
AbstractPlus | Full Text: PDF(256 KB) IEEE CNF
Rights and Permissions

27. **An iterative delay model for interconnects with coupling effects**
Zhaoran Yan; Xiaojun Guo; Huazhong Yang; Rong Luo; Hui Wang;
ASIC, 2003. Proceedings. 5th International Conference on
Volume 1, 21-24 Oct. 2003 Page(s):311 - 314 Vol.1
Digital Object Identifier 10.1109/ICASIC.2003.1277550
AbstractPlus | Full Text: PDF(326 KB) IEEE CNF
Rights and Permissions

28. **A comprehensive fault model for deep submicron digital circuits**
Abraham, J.A.; Krishnamachary, A.; Tupuri, R.S.;
Electronic Design, Test and Applications, 2002. Proceedings. The First IEEE International Worksho
29-31 Jan. 2002 Page(s):360 - 364
Digital Object Identifier 10.1109/DELTA.2002.994650
AbstractPlus | Full Text: PDF(222 KB) IEEE CNF
Rights and Permissions

29. **Gasping the impact of on-chip inductance**
Massoud, Y.; Ismail, Y.;
Circuits and Devices Magazine, IEEE
Volume 17, Issue 4, July 2001 Page(s):14 - 21
Digital Object Identifier 10.1109/101.950046
AbstractPlus | References | Full Text: PDF(2176 KB) IEEE JNL
Rights and Permissions

30. **Buffer delay change in the presence of power and ground noise**
Chen, L.H.; Marek-Sadowska, M.; Brewer, F.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 11, Issue 3, June 2003 Page(s):461 - 473
Digital Object Identifier 10.1109/TVLSI.2003.812310

AbstractPlus | References | Full Text: PDF(1001 KB) IEEE JNL
Rights and Permissions

☐ **31. An interconnect insensitive linear time-varying driver model for static timing analysis**
Chung-Kuan Tsai; Marek-Sadowska, M.;
Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium on
21-23 March 2005 Page(s):654 - 661
Digital Object Identifier 10.1109/ISQED.2005.16
AbstractPlus | Full Text: PDF(624 KB) IEEE CNF
Rights and Permissions

☐ **32. Modeling and propagation of noisy waveforms in static timing analysis**
Nazarian, S.; Pedram, M.; Tuncer, E.T.; Tao Lin; Ajami, A.H.;
Design, Automation and Test in Europe, 2005. Proceedings
2005 Page(s):776 - 777 Vol. 2
Digital Object Identifier 10.1109/DATE.2005.211
AbstractPlus | Full Text: PDF(144 KB) IEEE CNF
Rights and Permissions

☐ **33. CodSim - a combined delay fault simulator**
Wangqi Qiu; Xiang Lu; Zhuo Li; Walker, M.H.; Weiping Shi;
Defect and Fault Tolerance in VLSI Systems, 2003. Proceedings. 18th IEEE International Symposi
3-5 Nov. 2003 Page(s):79 - 86
AbstractPlus | Full Text: PDF(276 KB) IEEE CNF
Rights and Permissions

☐ **34. Proceedings Fourth International Symposium on Quality Electronic Design**
Quality Electronic Design, 2003. Proceedings. Fourth International Symposium on
24-26 March 2003
AbstractPlus | Full Text: PDF(337 KB) IEEE CNF
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WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Thursday, July 20, 2006

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ	
☐	L8	L6 and (model$ with (current or capacitance))	10
☐	L7	L6 and aggressor	3
☐	L6	L4 and model$	107
☐	L5	L4 and (crosstalk with delay) and model$	7
☐	L4	gate circuit and crosstalk and delay	305
☐	L3	L2 and (model same gate)	6
☐	L2	keller.in. and (gate with circuit) and delay	47
☐	L1	keller.in. and crosstalk and delay	2

END OF SEARCH HISTORY

Hit List

First Hit | Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 20050265473 A1

L1: Entry 1 of 2 File: PGPB Dec 1, 2005

PGPUB-DOCUMENT-NUMBER: 20050265473
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050265473 A1

TITLE: Method and device for processing received data of a radio interface

PUBLICATION-DATE: December 1, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Keller, Stefan	Freiburg		DE

US-CL-CURRENT: 375/267

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6049380 A

L1: Entry 2 of 2 File: USPT Apr 11, 2000

US-PAT-NO: 6049380
DOCUMENT-IDENTIFIER: US 6049380 A

TITLE: Single molecule identification using selected fluorescence characteristics

DATE-ISSUED: April 11, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Goodwin; Peter M.	Los Alamos	NM		
Jett; James H.	Los Alamos	NM		
Keller; Richard A.	Los Alamos	NM		
Van Orden; Alan K.	Los Alamos	NM		
Machara; Nicholas P.	Germantown	MD		

US-CL-CURRENT: 356/317; 250/458.1

Hit List

First Hit | Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 6 of 6 returned.

☐ 1. Document ID: US 20020194573 A1

L3: Entry 1 of 6 File: PGPB Dec 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020194573
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020194573 A1

TITLE: Method for simulating noise on the input of a static gate and determining noise on the output

PUBLICATION-DATE: December 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Keller, S. Brandon	Evans	CO	US
Rogers, Gregory D.	Fort Collins	CO	US

US-CL-CURRENT: 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20020190745 A1

L3: Entry 2 of 6 File: PGPB Dec 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020190745
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020190745 A1

TITLE: Method for calculating the P/N ratio of a static gate based on input voltages

PUBLICATION-DATE: December 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Keller, S. Brandon	Evans	CO	US
Rogers, Gregory D.	Fort Collins	CO	US

US-CL-CURRENT: 326/23

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6674247 B1

L3: Entry 3 of 6 File: USPT Jan 6, 2004

US-PAT-NO: 6674247
DOCUMENT-IDENTIFIER: US 6674247 B1

TITLE: Efficient photographic flash

DATE-ISSUED: January 6, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mead; Carver A.	Santa Clara	CA		
Keller; Glenn J.	Santa Cruz	CA		

US-CL-CURRENT: 315/241P; 315/200A, 315/241S

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 6502223 B1

L3: Entry 4 of 6 File: USPT Dec 31, 2002

US-PAT-NO: 6502223
DOCUMENT-IDENTIFIER: US 6502223 B1
** See image for Certificate of Correction **

TITLE: Method for simulating noise on the input of a static gate and determining noise on the output

DATE-ISSUED: December 31, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Keller; S Brandon	Fort Collins	CO		
Rogers; Gregory D.	Fort Collins	CO		

US-CL-CURRENT: 716/5; 716/16, 716/18, 716/4

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 5. Document ID: US 6496031 B1

L3: Entry 5 of 6 File: USPT Dec 17, 2002

US-PAT-NO: 6496031

DOCUMENT-IDENTIFIER: US 6496031 B1

TITLE: Method for calculating the P/N ratio of a static gate based on input voltages

DATE-ISSUED: December 17, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Keller; S Brandon	Evans	CO		
Rogers; Gregory D	Fort Collins	CO		

US-CL-CURRENT: 326/23; 326/121, 716/3

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 6. Document ID: US 3930120 A

L3: Entry 6 of 6 File: USPT Dec 30, 1975

US-PAT-NO: 3930120
DOCUMENT-IDENTIFIER: US 3930120 A

TITLE: Multi-beam cathode ray tube having equalized line brightness

DATE-ISSUED: December 30, 1975

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Keller; Bruce W.	Los Angeles	CA		
Hoffman; William C.	Torrance	CA		
Herman; Elvin E.	Pacific Palisades	CA		

US-CL-CURRENT: 348/206; 348/173

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
MODEL	597515
MODELS	194716
GATE	487031
GATES	227756
(2 AND (MODEL SAME GATE)).PGPB,USPT.	6
(L2 AND (MODEL SAME GATE)).PGPB,USPT.	6

Hit List

First Hit | Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: US 20050102594 A1

L5: Entry 1 of 7 File: PGPB May 12, 2005

PGPUB-DOCUMENT-NUMBER: 20050102594
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050102594 A1

TITLE: Method for test application and test content generation for AC faults in integrated circuits

PUBLICATION-DATE: May 12, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Dey, Sujit	San Diego	CA	US
Bai, Xiaoliang	La Jolla	CA	US
Chen, Li	Hillsboro	OR	US
Krstic, Angela	San Diego	CA	US

US-CL-CURRENT: 714/733

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20020133325 A1

L5: Entry 2 of 7 File: PGPB Sep 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020133325
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020133325 A1

TITLE: Discrete event simulator

PUBLICATION-DATE: September 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Hoare, Raymond R. II	Pittsburgh	PA	US
Ahn, Jiyong	Pittsburgh	PA	US
Graves, Jesse	Pittsburgh	PA	US

US-CL-CURRENT: 703/17

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 3. Document ID: US 6430731 B1

L5: Entry 3 of 7 File: USPT Aug 6, 2002

US-PAT-NO: 6430731
DOCUMENT-IDENTIFIER: US 6430731 B1

TITLE: Methods and apparatus for performing slew dependent signal bounding for signal timing analysis

DATE-ISSUED: August 6, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lee; Jin-Fuw	Yorktown Heights	NY		
Ostapko; Daniel Lawrence	Mahopac	NY		
Soreff; Jeffrey Paul	Poughkeepsie	NY		
Wong; Chak-Kuen	Shatin			HK

US-CL-CURRENT: 716/6; 716/4, 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 4. Document ID: US 6181596 B1

L5: Entry 4 of 7 File: USPT Jan 30, 2001

US-PAT-NO: 6181596
DOCUMENT-IDENTIFIER: US 6181596 B1

TITLE: Method and apparatus for a RAM circuit having N-Nary output interface

DATE-ISSUED: January 30, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Horne; Stephen C.	Austin	TX		
Seningen; Michael R.	Austin	TX		
Blomgren; James S.	Austin	TX		

US-CL-CURRENT: 365/168

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6118716 A

L5: Entry 5 of 7 File: USPT Sep 12, 2000

US-PAT-NO: 6118716
DOCUMENT-IDENTIFIER: US 6118716 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for an address triggered RAM circuit

DATE-ISSUED: September 12, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Horne; Stephen C.	Austin	TX		
Seningen; Michael R.	Austin	TX		
Blomgren; James S.	Austin	TX		

US-CL-CURRENT: 365/207; 365/196, 365/233.5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 6069836 A

L5: Entry 6 of 7 File: USPT May 30, 2000

US-PAT-NO: 6069836
DOCUMENT-IDENTIFIER: US 6069836 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for a RAM circuit having N-nary word line generation

DATE-ISSUED: May 30, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Horne; Stephen C.	Austin	TX		
Seningen; Michael R.	Austin	TX		
Blomgren; James S.	Austin	TX		

US-CL-CURRENT: 365/230.06; 365/189.08

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 6046931 A

L5: Entry 7 of 7 File: USPT Apr 4, 2000

US-PAT-NO: 6046931
DOCUMENT-IDENTIFIER: US 6046931 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for a RAM circuit having N-nary output interface

DATE-ISSUED: April 4, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Horne; Stephen C.	Austin	TX		
Seningen; Michael R.	Austin	TX		
Blomgren; James S.	Austin	TX		

US-CL-CURRENT: 365/168; 365/190, 365/207

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
CROSSTALK	28778
CROSSTALKS	610
DELAY	461074
DELAYS	158644
MODEL$	0
MODEL	597515
MODELA	22
MODELAA	3
MODELABBRV	1
MODELABILITIES	1
MODELABILITY	22
(L4 AND (CROSSTALK WITH DELAY) AND MODEL$).PGPB,USPT.	7

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 20060112357 A1

L7: Entry 1 of 3 File: PGPB May 25, 2006

PGPUB-DOCUMENT-NUMBER: 20060112357
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060112357 A1

TITLE: Sensitivity-current-based model for equivalent waveform propagation in the presence of noise for static timing analysis

PUBLICATION-DATE: May 25, 2006

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Nazarian; Shahin	South Pasadena	CA	US
Lin; Tao	Sunnyvale	CA	US
Tuncer; Emre	Santa Cruz	CA	US

US-CL-CURRENT: 716/4; 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. D

☐ 2. Document ID: US 20050102594 A1

L7: Entry 2 of 3 File: PGPB May 12, 2005

PGPUB-DOCUMENT-NUMBER: 20050102594
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050102594 A1

TITLE: Method for test application and test content generation for AC faults in integrated circuits

PUBLICATION-DATE: May 12, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Dey, Sujit	San Diego	CA	US
Bai, Xiaoliang	La Jolla	CA	US
Chen, Li	Hillsboro	OR	US
Krstic, Angela	San Diego	CA	US

US-CL-CURRENT: 714/733

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6587815 B1

L7: Entry 3 of 3 File: USPT Jul 1, 2003

US-PAT-NO: 6587815
DOCUMENT-IDENTIFIER: US 6587815 B1

TITLE: Windowing scheme for analyzing noise from multiple sources

DATE-ISSUED: July 1, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Aingaran; Kathirgamar	Sunnyvale	CA		
Haritsa; Manjunath D.	San Jose	CA		
Varadadesikan; Lakshminarasimhan	Santa Clara	CA		

US-CL-CURRENT: 703/13; 703/14, 703/15, 716/10, 716/2, 716/5, 716/6

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
AGGRESSOR	559
AGGRESSORS	212
(6 AND AGGRESSOR).PGPB,USPT.	3
(L6 AND AGGRESSOR).PGPB,USPT.	3

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Hit List

First Hit | Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 10 of 10 returned.

☐ 1. Document ID: US 20060112357 A1

L8: Entry 1 of 10 File: PGPB May 25, 2006

PGPUB-DOCUMENT-NUMBER: 20060112357
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060112357 A1

TITLE: Sensitivity-current-based model for equivalent waveform propagation in the presence of noise for static timing analysis

PUBLICATION-DATE: May 25, 2006

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Nazarian; Shahin	South Pasadena	CA	US
Lin; Tao	Sunnyvale	CA	US
Tuncer; Emre	Santa Cruz	CA	US

US-CL-CURRENT: 716/4; 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

☐ 2. Document ID: US 20050046584 A1

L8: Entry 2 of 10 File: PGPB Mar 3, 2005

PGPUB-DOCUMENT-NUMBER: 20050046584
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050046584 A1

TITLE: Asset system control arrangement and method

PUBLICATION-DATE: March 3, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Breed, David S.	Boonton Township	NJ	US

US-CL-CURRENT: 340/825.72; 280/735, 340/5.71, 455/420

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

☐ 3. Document ID: US 20050017488 A1

L8: Entry 3 of 10 File: PGPB Jan 27, 2005

PGPUB-DOCUMENT-NUMBER: 20050017488
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050017488 A1

TITLE: Weight measuring systems and methods for vehicles

PUBLICATION-DATE: January 27, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Breed, David S.	Boonton Township	NJ	US
DuVall, Wilbur E.	Kimberling City	MO	US
Johnson, Wendell C.	Signal Hill	CA	US

US-CL-CURRENT: 280/735

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 20040129478 A1

L8: Entry 4 of 10 File: PGPB Jul 8, 2004

PGPUB-DOCUMENT-NUMBER: 20040129478
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040129478 A1

TITLE: Weight measuring systems and methods for vehicles

PUBLICATION-DATE: July 8, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Breed, David S.	Boonton Township	NJ	US
DuVall, Wilbur E.	Kimberling City	MO	US
Johnson, Wendell C.	Signal Hill	CA	US

US-CL-CURRENT: 180/273; 280/735

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 5. Document ID: US 20030209893 A1

L8: Entry 5 of 10 File: PGPB Nov 13, 2003

PGPUB-DOCUMENT-NUMBER: 20030209893

PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030209893 A1

TITLE: Occupant sensing system

PUBLICATION-DATE: November 13, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Breed, David S.	Boonton Township	NJ	US
DuVall, Wilbur E.	Kimberling City	MO	US
Johnson, Wendell C.	Signal Hill	CA	US

US-CL-CURRENT: 280/735; 701/45

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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☐ 6. Document ID: US 20020133325 A1

L8: Entry 6 of 10 File: PGPB Sep 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020133325
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020133325 A1

TITLE: Discrete event simulator

PUBLICATION-DATE: September 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Hoare, Raymond R. II	Pittsburgh	PA	US
Ahn, Jiyong	Pittsburgh	PA	US
Graves, Jesse	Pittsburgh	PA	US

US-CL-CURRENT: 703/17

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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☐ 7. Document ID: US 7039536 B2

L8: Entry 7 of 10 File: USPT May 2, 2006

US-PAT-NO: 7039536
DOCUMENT-IDENTIFIER: US 7039536 B2

TITLE: Method and apparatus for analyzing a source current waveform in a semiconductor integrated circuit

DATE-ISSUED: May 2, 2006

PRIOR-PUBLICATION:

DOC-ID	DATE
US 20020147555 A1	October 10, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nagata; Makoto	Hiroshima			JP
Iwata; Atsushi	Hiroshima			JP

US-CL-CURRENT: 702/70; 702/64, 702/66, 703/14, 716/4

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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☐ 8. Document ID: US 6841950 B1

L8: Entry 8 of 10 File: USPT Jan 11, 2005

US-PAT-NO: 6841950
DOCUMENT-IDENTIFIER: US 6841950 B1

TITLE: Dimmable electrolumanescent lamp drivers and method therefor

DATE-ISSUED: January 11, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Walker; James T.	Palo Alto	CA		

US-CL-CURRENT: 315/169.3; 315/209R, 315/291, 315/312, 315/DIG.4, 323/218, 323/233

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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☐ 9. Document ID: US 6587815 B1

L8: Entry 9 of 10 File: USPT Jul 1, 2003

US-PAT-NO: 6587815
DOCUMENT-IDENTIFIER: US 6587815 B1

TITLE: Windowing scheme for analyzing noise from multiple sources

DATE-ISSUED: July 1, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Aingaran; Kathirgamar	Sunnyvale	CA		
Haritsa; Manjunath D.	San Jose	CA		
Varadadesikan; Lakshminarasimhan	Santa Clara	CA		

US-CL-CURRENT: 703/13; 703/14, 703/15, 716/10, 716/2, 716/5, 716/6

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 10. Document ID: US 6253361 B1

L8: Entry 10 of 10 File: USPT Jun 26, 2001

US-PAT-NO: 6253361
DOCUMENT-IDENTIFIER: US 6253361 B1

TITLE: Generalized theory of logical effort for look-up table based delay models using capacitance ratio

DATE-ISSUED: June 26, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Buch; Premal	Daly City	CA		

US-CL-CURRENT: 716/6

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
CURRENT	1551605
CURRENTS	227363
CAPACITANCE	208519
CAPACITANCES	43070
MODEL$	0
MODEL	597515
MODELA	22
MODELAA	3
MODELABBRV	1
MODELABILITIES	1
MODELABILITY	22
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